Synchronization and Power Integrity Issues in 3-D ICs

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***Abstract*— Several challenges should be resolved for three-dimensional integration to evolve to a mainstream technology. Among these challenges, the issues of synchronization and power integrity become predominant due to the multiple planes and the heterogeneity of 3-D circuits. The paper offers an overview of the state of the art research related to these global in nature issues. Experimental results, design techniques, and models are discussed highlighting the possible means and requirements for the design of reliable synchronization and power distribution schemes in 3-D circuits.**

***Keywords*— 3-D integration, synchronization, clock distribution networks, power distribution networks.**

I. Introduction

Vertically integrated circuits are considered a potent design paradigm to overcome the many limitations of modern planar circuits. The shorter interconnects and diversity of functions are the salient traits of this emerging technology [1]. Stacking physical planes and integrating dissimilar circuits, however, complicates specific design tasks. These tasks include floorplanning, placement, and routing as well as global physical design issues, such as synchronization and power distribution [2]. The complexity of the functions and the disparity of technologies that 3-D circuits are forecasted to encompass, require reconsidering the way that these issues have been addressed to date.

A key element of any three-dimensional technology is the vertical interconnects that support the communication among circuits located on different physical planes. These interconnects are primarily implemented with through silicon vias (TSVs) [3], [4]. Although contactless communication schemes among the planes have been demonstrated [5], the discussion herein focuses on TSV-based 3-D systems.

The impedance and physical characteristics of the TSVs considerably differ from the typical horizontal metal wires used for intraplane connections [6]. Consequently, these new interconnect structures affect differently, the signal delay in the vertical direction and also contribute to the power supply noise of a 3-D power distribution network.

Another important requirement for 3-D systems is the ability to functionally test each plane prior and post bonding. This requirement adds new difficulties in providing the proper clock distribution network within each plane and throughout the entire 3-D circuit.

The desired heterogeneity of 3-D systems, which appears as a driving force for this type of systems also calls for more complex clocking and power delivery strategies. Novel and not fully synchronous approaches can be other promising synchronization mechanisms for 3-D systems.

The aforementioned argument also applies for power delivery in 3-D circuits. The traditional hierarchy of a power distribution system from the off-chip voltage regulator module to the on-chip power distribution network should be revised to provide abundant current to the circuits within all planes.

The thermal behaviour of 3-D circuits also poses changes in traditional clock and power distribution design. This situation is due to the increase in the resistance of the wires due to the elevated temperatures and the increased power densities due to circuit stacking. In addition, the efficient thermal management of 3-D systems can employ a mixture of techniques at the system, architecture, and physical level. At the system level, the use of typical voltage and frequency scaling techniques in planar techniques is further extended in 3-D circuits to mitigate hot spots and growing thermal gradients; particularly for envisaged multi-processor 3-D systems. Consequently, 3-D power delivery schemes should provide several voltage levels at a fine granularity.

Measurements from a 3-D test circuit and clock synthesis techniques are reviewed in the following section. Additionally, the effect of process variations on specific 3-D clock distribution networks is discussed. The less explored issue of power integrity is analysed in Section III, where possible solutions for the design of power distribution networks and on-chip power generators are demonstrated.

II. Synchronization in 3-D Circuits

In principle, efficient synchronization consists of two basic tasks; clock generation and clock distribution, the latter being the focus of this section. There are a few ramifications in designing a robust clock distribution network for 3-D circuits. These design implications are described in this section.

The primary objective in synchronous 3-D circuits is to reliably propagate the clock signal within each plane and throughout the planes of the 3-D stack. The additional difficulty in performing this task as compared to planar circuits is due to several reasons. For example, the two different types of interconnects employed in these circuits; the TSVs and the intraplane wires. In addition, the introduction of the third dimension can render common planar topologies less effective. Furthermore, the variability of devices within 3-D circuits comprises different sources of process variations, the effect of which should be considered in the design of multi-plane clock distribution networks.

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Several electrical models for the vertical interconnects have recently been presented [4], [6]. Note that the electrical characteristics of the TSVs are strongly linked to the target manufacturing technology. To explore the effect of the TSVs on 3-D clock distribution networks, a prototype 3-D circuit has been fabricated with the MIT Lincoln Labs bonding technology [7]. The circuit employs several candidate topologies for globally distributing the clock signal within a 3-D circuit depicted in Fig. 1. For instance, a topology consists of an H-tree in each plane and all trees are connected with a group of TSVs at the root of the trees (see Fig. 1a). Another possible topology includes an H-tree in the middle plane (due to symmetry purposes) and local meshes connected with TSVs to the leaves of the tree in the other planes, as shown in Fig. 1b.

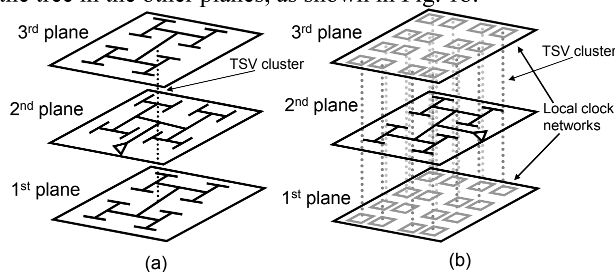

Fig. 1. Schematic of candidate 3-D clock distribution networks, (a) replicated H-trees and (b) multi-via H-tree topology.

Experimental results from the test circuit indicate that TSVs for this specific technology contribute a low overhead in clock delay. Furthermore, the clock skew is not excessive. In addition, correct operation at gigahertz frequencies is demonstrated, which is an encouraging result for developing 3-D technologies. The limitations of these global topologies, however, is that the short and, consequently, low latency TSVs are not fully explored. Additionally, assuming that testing each plane prior to bonding is a prerequisite for high yield, each of these topologies can require a large number of probing points across each plane [8]. This situation can increase the difficulty in designing these topologies.

In an effort to respond to the testing challenge, a clock synthesis technique is proposed in [9]. This technique produces two clock networks, each of which is used prior (for testing) and post (for normal operation) bonding. The overhead for the improved testability is a moderate increase in power consumed by the clock distribution network.

A fundamental notion of 3-D integration is that by increasing the number of planes, the clock frequency can monotonically increase, following the reduction in wirelength [10]. The variability of clock skew within a 3-D circuit is shown not to always exhibit the same behaviour. To explain this different behaviour, consider that each plane is subjected to different types of process variations; die-to-die (D2D) and within-die (WID) variations. Inter-die variations affect the characteristics of devices independently among planes, but the devices within one plane are uniformly affected. Intra-die variations affect the characteristics of devices unequally within one die. 3-D integration can be effective in mitigating the impact of process variations as compared to 2-D designs [11]. This improvement is demonstrated for different datapaths. Considering the common segments of the 3-D clock paths (a situation that does not typically apply to datapaths) and both the D2D and WID process variations, the effect of process variations on clock skew in 3-D ICs is investigated in [12].

The topologies shown in Fig. 1 propagate the clock signal at the same points within a 3-D circuit. The length of the segments shared by the paths within these networks differs considerably. The overall effect of the process fluctuations, therefore, on the variability of clock skew varies.

In both cases, the standard deviation (σ) of skew is shown to change non-monotonically with the number of planes. Briefly, σ of skew within a plane is decreased by the topology illustrated in Fig. 1a, while the σ of skew between different planes is reduced by the multi-via topology plotted in Fig. 1b. To efficiently alleviate both sources of variations a hybrid H-tree topology is proposed. The variability of skew is shown to decrease where the registers within the circuit are properly partitioned. In Fig. 2, the registers that store data in common datapaths are assumed to be placed in two different groups of planes, each driven by an individual H-tree topology.

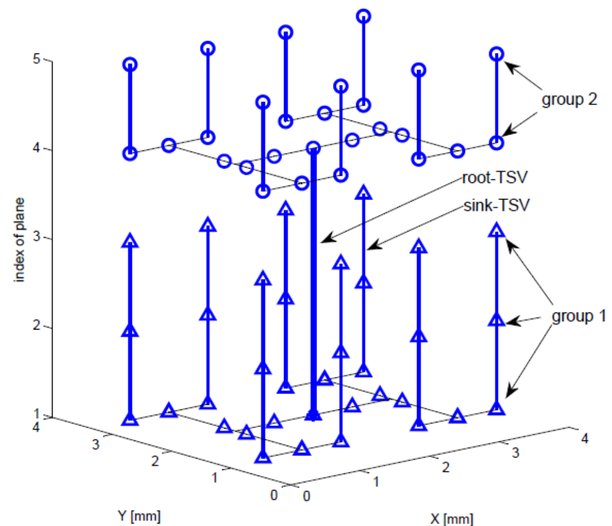

Fig. 2. Hybrid H-tree topology, where the careful partition of the circuit can decrease the pairwise skew variation within a 3-D circuit.

In addition to process variations, circuit switching and interconnect joule heating can result in considerable temperature fluctuations across the area of an integrated circuit [13]. These fluctuations, in turn, can affect the clock delay along different paths within the circuit resulting in deviations of the nominal clock skew. This behaviour can be further pronounced in 3-D circuits due to the increased power densities throughout the stacked planes. To mitigate the spatial thermal gradients across planes, a circuit technique presented in [14] can be applied.

Another important source of variations is the voltage variations that arise from the abrupt current transients that can be produced within a circuit. The most efficient means to curtail

these voltage variations is a properly designed power distribution network. The challenges related to this task are discussed in the following section.

III. Power Integrity in 3-D ICs

The important advantage of reduced footprint, which improves the speed and the form factor of a 3-D system, can simultaneously degrade the power integrity of these systems. The underlying reason is the decreased area of the circuit, which leads to a higher current density and a lower number of power/ground (P/G) pads. In addition, this current for all but one of the planes in the 3-D stack has to be delivered by the TSVs. To guarantee adequate current within a 3-D circuit, consequently, is not straightforward. The lack of design automation tools further impedes the design of proper and not highly overdesigned 3-D power distribution networks.

To date there are few efforts to capture the effects of the impedance characteristics on the power supply noise in 3-D circuits [15]. Analytic models of reasonable accuracy have also been developed [16], [17]. The primary assumption and, at the same time, limitation of these models is the consumption of uniform current density in all or across each plane. Although this approach, simplifies the modelling process, having a uniform power demand among planes is rather unlikely. The usefulness of these models, however, is that specific behaviours can be depicted. For example, the importance of the TSV density in a 3-D system is demonstrated in [17].

Alternatively, an improved model for guiding the design process of 3-D power distribution networks should relate the physical design parameters with the resulting voltage drop. These parameters can, for example, include the width of the P/G lines and the number of P/G pairs of lines across the metal layers of a plane. Additionally, the effect between the area occupied by the TSVs and the intraplane wiring resources should be considered. To this end, employing a uniform distribution of TSVs and similar power grids in each plane, the resistive voltage drop at the load within plane p of a 3-D system can be described as

$$V_{L,p} = V_{Power_Supply} - \left[\sum_{k=p}^{N_p-1} kI_{cell}R_{TSV}\right] - I_{cell}R_{p-plane}, \quad (1)$$

where I_{cell} is the current drawn within a cell formed by four neighbouring pairs of P/G TSVs and R_{TSV} is the resistance of a TSV from [4]. The intraplane resistance of the power grid from the TSV to the load within the cell is written as,

$$R_{p-plane} = \frac{\rho\sqrt{A_{cell}}}{N_{p,M_p}W_{p,M_p}H_{p,M_p}} + \sum_{1}^{M_p-1}\left(\frac{\rho P_{p,n+1}}{2W_{p,n}N_{p,n}H_{p,n}N_{p,n+1}} + \frac{R_{via}}{N_{p,n}N_{p,n+1}}\right), \quad (2)$$

where n denotes the nth metal layer in plane p and $n_{max} = M_p$ as determined by the target technology. The physical design parameters of the P/G lines; namely, pitch, spacing, width, and thickness are denoted as $P_{p,n}$, $S_{p,n}$, $W_{p,n}$, and $H_{p,n}$, respectively. The number of P/G pairs within a cell is given by $N_{p,n}$. Finally, the current I_{cell} is a linear function of the density of the TSVs within the 3-D circuit. By employing this model, the interplay among the different interconnect resources can be explored.

As a case study consider a 3-D circuit consisting of ten planes with a plane area of 2 cm × 2 cm. The physical parameters of the TSVs are the diameter, length, and surrounding dielectric thickness which are equal to 5 μm, 100 μm, and 50 nm, respectively. Following the ITRS predictions for a 45 nm technology node [18], the current demand and power supply are 64 A/cm^2 and 1.1 Volts, respectively. Assuming typical sizes for the P/G lines and allowed voltage drop of 5% V_{dd} at the load, the design space where this constraint is satisfied is the crosshatched area illustrated in Fig. 3. This design space is defined by different contours of the area allocated to TSVs, A_{TSV} and the power grids, A_{PDN} given as percentages of the plane area A_c.

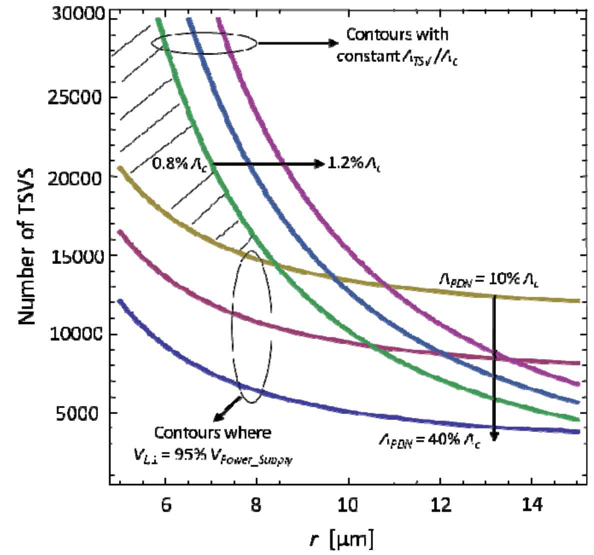

Fig. 3. Design space defined by the contour plots $V_{L,1} = 0.95V_{Power_Supply}$ where the TSV number (y-axis) and diameter (x-axis) are varied such that the ratio A_{TSV}/Ac is constant. This design space varies as a function of the area allocated to the intra-plane power distribution network and the area occupied by the TSVs, as illustrated by the arrows.

Intuitively, by increasing either type of the metal resources decreases the resistive voltage drop. Increasing the area of the TSVs lowers both the current demand within a cell and the impedance of the power distribution network in the vertical direction. The contribution of the power grid resources, however, is greater as shown by the corresponding family of curves in Fig. 3.

The model described by (1) and (2) links the physical design characteristics of the power grids and the TSVs with the resistive voltage drop throughout a stack of planes. The inductive component of the power supply noise, however, is not explicitly captured. The effect of the *Ldi/dt* noise in the investigated 3-D circuit is a decrease in the design space depicted in Fig. 3.

An efficient means to improve power integrity in integrated circuits has traditionally been the use of decoupling capacitance. A recent method to allocate metal-insulator-metal (MIM) and typical MOS capacitors in 3-D circuits is proposed in [19]. The objective of the method is to satisfy the specified voltage drop constraints, while not increasing significantly the routing congestion (due to MIM capacitors) and not exceeding the available area (due to the MOS capacitors). To achieve this objective a balanced distribution of these two types of capacitance is required. The objective function is augmented with proper coefficients that control the allocation of either MIM or MOS capacitance within the 3-D circuit. A sequence of linear programs is utilized to satisfy the required objective. Application of the method on benchmark circuits [20] demonstrates that a combination of MIM and MOS capacitors results in lower leakage current and routing congestion due to the decoupling capacitors while respecting the area constraints.

In addition to power distribution, the power delivery task is also of significant importance. Since 3-D circuits are forecasted to require aggressive voltage scaling mechanisms to moderate thermal gradients and hot spots, multiple voltage domains are required. This requirement is further aggravated by the possibility to integrate an analog plane, which typically exploits different power supply levels as compared to the digital planes.

To address these needs, a multi-story power delivery system is proposed [21]. The multi-plane nature of 3-D circuits suits such a scheme. The fundamental idea of this approach is that the number of supply levels is equal to the number of planes. For example, in the nth plane two power supply rails nV_{dd} and $(n\text{-}1)V_{dd}$ are used. The voltage difference seen at the P/G lines is V_{dd}. This technique has been shown to improve the voltage drop and remains useful when the current consumption within each plane is the same. In this manner, the current drawn from one plane is fed to the subsequent plane, lowering the overall power consumption. Current balancing, however, is a considerable challenge for this approach.

Alternatively, the demand for multi-voltage domains can be satisfied by the on-chip distribution of small and efficient DC-DC converters. These circuits can supply with current small regions in a plane or between planes, forming several voltage islands. Some area efficient designs of these converters have recently appeared [22]. The primary advantage of these designs is the elimination of the bulky inductors, thereby being suitable for miniaturized volumetric integrated systems.

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